REMARKS

Applicant thanks the Examiner for the Interview held on June 3, 2005 and withdrawing the statutory double patenting rejection.

Claims 1-7, 9, and 11-20 are pending. Reconsideration and allowance of the claims in view of the above amendments and the remarks that follow are respectfully requested.

Allowable Subject Matter

Applicant thanks the Examiner for indicating that claims 1-7, 9, and 11-20 contain allowable subject matter. Applicant respectfully comments that the claims are allowable for features they recite, singularly and/or in combination. Additional features and combinations thereof, beyond those mentioned on page 3 of the May 13, 2005 Office Action, are not found or suggested in the prior art.

Statutory Double Patenting Rejections

Claim 1 is rejected under 35 U.S.C. §171 on the ground of statutory double patenting over claim 1 of U.S. Patent 6,581,197 (application no. 09/927,856 filed August 10, 2001) (hereafter the '197 patent). Applicant thanks the Examiner for withdrawing the statutory double patenting rejection during the June 3, 2005 Interview.

Obviousness Double Patenting Rejections

Claim 1 is rejected under the judicially created doctrine of obviousness-type double patenting over claim 1 of the '197 patent. This rejection is respectfully traversed.

The present application (09/927,204) is directed to a method and apparatus for verifying a minimal level sensitive timing abstraction model. The method modifies and runs the timing abstraction model with certain stimulus to establish whether the timing results with the timing abstraction model are identical to the timing result with a modeled circuit. The method identifies relevant timing paths in the echo-circuit, identifies paths in the modeled circuit that connect sequential elements and correspond to the relevant timing paths in the echo-circuit, and compares the relevant timing paths in the echo-circuit with the corresponding paths in the modeled circuit.

On the other hand, the '197 patent is directed to a minimal level sensitive timing representative of a circuit path. The echo-circuit recited in the '197 patent models a single circuit path by maintaining clock edges of a first latch at an input port and last latch at an output port, which does not involve verifying the timing abstraction model by identifying relevant timing paths in the echo-circuit, identifying paths in the modeled circuit that connect sequential elements and correspond to the relevant timing paths in the echo-circuit, and comparing the relevant timing paths in the echo-circuit with the corresponding paths in the

modeled circuit. Therefore, Applicant respectfully submits that the present application and the '197 patent are patentably distinct.

However, in the interest of efficiency, a terminal disclaimer is filed herewith in order to place the application in condition for allowance. Prompt examination and allowance are respectfully requested.

Should the Examiner believe that anything further is desired in order to place the application in even better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

Date: **June 6, 2005**

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Attachment: Terminal Disclaimer